This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Currently amended) A method for fabricating an RF semiconductor device comprising:

forming a trench to define an active region and an element isolation region in a semiconductor substrate;

forming ~~at least one gate line~~ a plurality of gate lines within the active region of the semiconductor substrate, the ~~at least one gate line~~ plurality of gate lines not extending over a center of the trench;

forming an insulating layer on the ~~at least one gate line~~ plurality of gate lines and the semiconductor substrate;

forming ~~a~~ at least one contact hole in the insulating layer within the active region without forming a contact hole within the element isolation region;

forming a contact plug in the contact hole; and

forming a conductive pattern layer that is electrically connected with the contact plug.

2. (Currently amended) A method as defined in claim 1, wherein ~~the at least one gate line comprises at least two gate lines, and the at least two~~ plurality of gate lines are not connected with each other in the element isolation region

3. (Currently amended) A method as defined in claim [[2]] 1, wherein at least two of the ~~at least two~~ plurality of gate lines are connected in the active region.

4. (Original) A method as defined in claim 1, wherein a thickness of the insulating layer is about 1000 to about 20000 angstroms.

5. (Original) A method as defined in claim 1, wherein a thickness of the conductive pattern layer is above 10000 angstroms.

6. (Currently amended) A method as defined in claim 1, wherein the insulating layer is one of ~~a low temperature~~ an oxide and a polyimide.

7. (Currently amended) A method as defined in claim 1, wherein the ~~at least one gate line is~~ plurality of gate lines are formed in order to minimize parasitic capacitance between the ~~at least one gate line~~ plurality of gate lines and the substrate.

8. (Currently amended) A method as defined in claim 1, wherein the ~~at least one gate line is~~ plurality of gate lines are formed in order to minimize resistance of the ~~at least one gate line~~ plurality of gate lines.

9. (Currently amended) A method as defined in claim 1, ~~furthur~~ further comprising metal contacts linking at least two of the plurality of ~~at least one~~ gate lines.

10. (Currently amended) A method as defined in claim 1, wherein the ~~at least one gate line does not~~ plurality of gate lines do not extend along a longitudinal axis of the trench.

11. (Canceled)

12. (Canceled)

Please add the following new claim:

13. An RF semiconductor device comprising:

a substrate;

first and second trenches defining an active region and at least one isolation region in the substrate, the first and second trenches being located on opposite sides of the active region, each of the first and second trenches having a longitudinal axis; and

a plurality of gate lines formed in the active region and oriented substantially perpendicularly to the longitudinal axes of the first and second trenches, wherein the gate lines do not extend along the longitudinal axes of the first and second trenches.

14. An RF semiconductor device comprising:

a substrate;

first and second trenches defining an active region and at least one isolation region in the substrate, the first and second trenches being located on

opposite sides of the active region; and

at least two gate lines extending across the active region from the first trench to the second trench without passing above a center of either of the first and second trenches.